What is Claimed is:

1. An isolation structure for a semiconductor assembly comprising:

a first trench in a semiconductive substrate;
a second trench extending the overall trench depth in said semiconductive substrate by being aligned to said first trench;
an insulation material substantially filling said first and second trenches.

2. The isolation structure as recited in claim 1, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

3. The isolation structure as recited in claim 1, wherein said first trench is lined with a dielectric material that is the same type of material as said insulation material.

4. The isolation structure as recited in claim 1, wherein said first trench is lined with a dielectric material that is chemically different than said insulation material.

5. The isolation structure as recited in claim 4, wherein said dielectric material comprises nitride and said insulation material comprises oxide.

6. The isolation structure as recited in claim 1, wherein said semiconductive substrate comprises silicon.

7. An isolation structure for a semiconductor assembly comprising:

a first trench in a semiconductive substrate;
a second trench extending the overall trench depth in said semiconductive substrate by being aligned to said first trench;
a planarized insulation material substantially filling said first and second trenches.

8. The isolation structure as recited in claim 7, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

9. The isolation structure as recited in claim 7, wherein said first trench is lined with a dielectric material that is the same type of material as said insulation material.

10. The isolation structure as recited in claim 7, wherein said first trench is lined with a dielectric material that is chemically different than said insulation material.

11. The isolation structure as recited in claim 10, wherein said dielectric material comprises nitride and said insulation material comprises oxide.

12. The isolation structure as recited in claim 7, wherein said semiconductive substrate comprises silicon.

13. A semiconductor assembly having at least one isolation structure comprising:

a first trench in a semiconductive substrate;
a second trench extending the overall trench depth in said semiconductive substrate by being aligned to said first trench;
an insulation material substantially filling said first and second trenches;
said isolation structure separating a non-continuous surface of a conductive region.

14. The isolation structure as recited in claim 13, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

15. The isolation structure as recited in claim 13, wherein said first trench is lined with a dielectric material that is the same type of material as said insulation material.

16. The isolation structure as recited in claim 13, wherein said first trench is lined with a dielectric material that is chemically different than said insulation material.

17. The isolation structure as recited in claim 16, wherein said dielectric material comprises nitride and said insulation material comprises oxide.

18. The isolation structure as recited in claim 13, wherein said semiconductive substrate comprises silicon.

19. A semiconductor assembly having at least one isolation structure comprising:

a first trench in a semiconductive substrate;
a second trench extending the overall trench depth in said semiconductive substrate by being aligned to said first trench;
a planarized insulation material substantially filling said first and second trenches;
said isolation structure separating a non-continuous surface of a conductive region.

20. The isolation structure as recited in claim 19, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

21. The isolation structure as recited in claim 19, wherein said first trench is lined with a dielectric material that is the same type of material as said insulation material.

22. The isolation structure as recited in claim 19, wherein said first trench is lined with a dielectric material that is chemically different than said insulation material.

23. The isolation structure as recited in claim 22, wherein said dielectric material comprises nitride and said insulation material comprises oxide.

24. The isolation structure as recited in claim 19, wherein said semiconductive substrate comprises silicon.

25. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;
forming a dielectric lining on the surface of said first trench;
forming a spacer along the sidewall of said first trench;
forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;
forming an insulative material in said first and second trenches, said insulative material substantially filling said first and second trenches.

26. The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

27. The process as recited in claim 25, wherein said spacer is formed from an oxidizable material.

28. The process as recited in claim 25, wherein said spacer is formed of oxide.

29. The process as recited in claim 25, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

30. The process as recited in claim 25, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same material.

32. The process as recited in claim 31, wherein said dielectric lining inhibits becoming oxidized.

33. The process as recited in claim 25, wherein said process uses only one mask to form said device isolation.

34. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;
forming a dielectric lining on the surface of said first trench;
forming a semiconductive spacer along the sidewall of said first trench;
forming a second trench into said semiconductor substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide;
forming an insulative material in said first and second trenches, said insulative material substantially consuming said semiconductive spacer and thereby substantially filling said first and second trenches;
planarizing said insulative material;

wherein said process uses only one mask to form said device isolation.

35. The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

36. The process as recited in claim 34, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

37. The process as recited in claim 34, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. The process as recited in claim 34, wherein said insulative material and said dielectric lining are the same material.

39. The process as recited in claim 34, wherein said dielectric lining inhibits becoming oxidized.

40. A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;
forming a first trench into said silicon substrate assembly using said mask as an etching guide;
forming an oxide layer on the surface of said first trench;
forming a silicon spacer on the sidewall of said first trench;
forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;
forming an oxide filler in said first and second trenches, said oxide substantially consuming said silicon spacer and thereby substantially filling said first and second trenches;
planarizing said oxide filler.

41. The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

42. The process as recited in claim 40, further comprising the step of forming an insulation layer, comprising oxide and nitride, on said semiconductor substrate prior to said step of forming a first trench.

43. The process as recited in claim 40, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

44. The process as recited in claim 40, further comprising the step of:

forming a conformal layer of polysilicon into said first and second trenches prior to said step of forming an oxide filler.

45. A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;
forming a first trench into said silicon substrate assembly using said mask as an etching guide;
forming a nitride layer on the surface of said first trench;
forming a silicon spacer on the sidewall of said first trench;
forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;
forming an oxide filler in said first and second trenches, said oxide substantially consuming said silicon spacers and thereby substantially filling said first and second trenches;
planarizing said oxide filler.

46. The process as recited in claim 45, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

47. The process as recited in claim 45, further comprising the step of forming an oxide layer on said semiconductor substrate prior to said step of forming a first trench.

48. The process as recited in claim 45, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

49. The process as recited in claim 45, further comprising the step of:

forming a conformal layer of polysilicon into said first and second trenches prior to said step of forming an oxide filler.

50. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate;
forming a dielectric lining on the surface of said trench;
forming a semiconductive spacer along the sidewall of said trench;
forming an insulative material in said trench, said insulative material substantially consuming said semiconductive spacer and thereby substantially filling said trench.

51. The process as recited in claim 50, wherein an overall depth of said trench is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

52. The process as recited in claim 50, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a trench.

53. The process as recited in claim 50, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. The process as recited in claim 50, wherein said insulative material and said dielectric lining are the same material.

55. The process as recited in claim 50, wherein said dielectric lining inhibits becoming oxidized.

56. The process as recited in claim 50, wherein said process uses only one mask to form said device isolation.